REMARKS

Claims 1-45, 47-56, 58-68, and 70-72 are now pending in the application. Claims 46, 57, and 69 are cancelled without disclaimer or prejudice to the subject matter contained therein. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 22, 23, 25, 29, 32, and 34 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nagaraj et al. (U.S. Pat. No. 5,642,077). This rejection is respectfully traversed.

With respect to claim 22, Nagaraj fails to show, teach, or suggest analog integrated function means for providing first and second output signals responsive to a first differential input signal pair and a second differential input signal pair. In particular, Nagaraj fails to disclose the limitation of first and second output signals responsive to **first and second differential input signal pairs**.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Nagaraj fails to disclose the limitation of providing first and second output signals responsive to a first differential input signal pair and a second differential input signal pair.

As shown in an exemplary embodiment in FIG. 4a of the present application, an analog function circuit receives a first differential input signal pair (i.e. the pair of inputs V_X) and a second differential input signal pair (i.e. the pair of inputs V_Y). The analog function circuit provides first and second output signals in response to the first differential input signal pair V_X and the second differential input signal pair V_Y.

Nagaraj does not appear to disclose this limitation. The Examiner relies on FIG. 1 of Nagaraj to disclose analog integrated function means (elements 122, 120, 140, and 104). Applicant respectfully notes that the alleged analog integrated function means does not provide first and second output signals responsive to **first and second differential input signal pairs** as claim 22 recites. In other words, Applicant's claim 22 recites **two pairs** of differential input signals (i.e. two differences between respective pairs of inputs V_X and V_Y as shown in FIG. 4a). As best understood by Applicant, Nagaraj discloses only a single differential input signal pair.

Applicant respectfully submits that claim 22, as well as its dependent claims, should be allowable for at least the above reasons. Claim 32, as well as its dependent claims, should be allowable for at least similar reasons.

REJECTION UNDER 35 U.S.C. § 103

Claims 31 and 45-72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagaraj et al. (U.S. Pat. No. 5,642,077). This rejection is respectfully traversed.

With respect to claim 45, Nagaraj fails to disclose a biasing circuit in communication with a common mode node of the differential loading device and an

input of the compensation circuit that provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and that provides a plurality of control bias voltage signals to the compensation circuit.

It is a longstanding rule that to establish a prima facie case of obviousness of a claimed invention, all of the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 143 (CCPA 1974), see MPEP §2143.03. Here, the Examiner fails to provide **any** reference to support a finding that a bias circuit that provides a common mode voltage **and** a plurality of control bias voltage signals is obvious. Furthermore, when evaluating claims for obviousness under 35 U.S.C. §103, all of the limitations must be considered and given weight. *Ex parte Grasselli*, 231 USPQ 393 (Bd. App. 1983), MPEP § 2144.03. Here, it is clear that the Examiner has given little or no consideration of the limitation **and failed to give the limitation any weight**.

Applicant respectfully notes that Nagaraj does not explicitly disclose or show a biasing circuit. Instead, the Examiner maintains that a biasing circuit provides the common mode voltage V_{CM}. In other words, the Examiner appears to allege that the biasing circuit is implicit. To the contrary, Applicant respectfully asserts that the alleged biasing circuit is not shown and, as such, the Examiner's reliance on the alleged biasing circuit to disclose specific claim elements is improper.

For example, claim 45 recites that the biasing circuit provides **the common mode voltage and a plurality of control bias voltage signals**. As shown in an exemplary embodiment in FIG. 4a of the present application, a bias circuit provides a

common mode voltage Vcm and a plurality of control bias voltage signals Vc1, Vc2, and Vc3.

The Examiner alleges that the undisclosed biasing circuit of Nagaraj provides the common mode voltage V_{CM} and a supply voltage V_{DD} to the alleged compensation circuit. Applicant respectfully disagrees. Nagaraj is absent of any description of an actual biasing circuit. Applicant respectfully notes that there is no support or evidence for the Examiner's allegation that the same circuit provides both the common mode voltage V_{CM} and the supply voltage V_{DD}.

Applicant further notes that even if the same circuit in Nagaraj (e.g. the alleged biasing circuit) provided both the common mode voltage V_{CM} and the supply voltage V_{DD}, Nagaraj still fails to disclose that the circuit provides **a plurality of control bias voltage signals to the compensation circuit**. The Examiner relies on the common mode voltage signal V_{CM} and the supply voltage V_{DD} to disclose the plurality of control bias voltage signals. In other words, the Examiner relies on the common mode voltage signal V_{CM} to disclose the common mode voltage signal and one of the plurality of control bias voltage signals.

Here again, Applicant respectfully notes that claim 45 recites that the biasing circuit provides both the common mode voltage signal **and** the plurality of control bias voltage signals to the compensation circuit. In other words, the plurality of control bias voltage signals are provided in addition to the common mode voltage signal. As such, the Examiner's reliance on the common mode voltage signal V_{CM} to disclose both the common mode voltage signal and one of the plurality of control bias voltage signal of Applicant's claim 45 is improper.

In view of the foregoing, Applicant respectfully submits that claim 45, as well as its dependent claims, should be allowable for at least the above reasons. Claims 56 and 67, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

ALLOWABLE SUBJECT MATTER

Claims 1-21 and 41-44 are allowed. The Examiner states that claims 26-28, 30, and 35-40 would be allowable if rewritten in independent form. Applicant thanks the Examiner for the allowable subject matter. Applicant elects to defer amending these claims into independent form until after the Examiner considers the above remarks.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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